IN THE CLAIMS:

Claims 15, 19, 36, 57 and 77 were previously cancelled. Claims 13, 54, 62, 76, 79, 92 and 115 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Previously presented) A semiconductor device package, comprising:

a semiconductor die with a plurality of bond pads arranged on an active surface thereof;

a tape positioned over the active surface, the tape including at least one slot formed therethrough, each of the plurality of bond pads being exposed through the at least one slot, at least one end of the at least one slot extending beyond an outer periphery of the semiconductor die;

a substrate element positioned over the tape opposite the semiconductor die, the substrate element including a plurality of contact areas, each contact area of the plurality corresponding to a bond pad of the plurality of bond pads and electrically connected thereto by way of an intermediate conductive element that extends through at least one opening formed through the substrate element and aligned with the at least one slot of the tape, the substrate element further including a contact pad in communication with each contact area of the plurality of contact areas by way of a substantially laterally extending conductive trace;

a quantity of encapsulant material substantially filling a volume defined by the at least one slot of the tape and the at least one opening of the substrate element; and

a coverlay secured to a surface of the substrate element opposite the tape, the coverlay substantially covering at least the at least one opening through the substrate element, contact pads of the substrate element being exposed beyond or through the coverlay.

2. (Previously presented) The semiconductor device package of claim 1, wherein the plurality of bond pads is arranged substantially linearly along a central region of the active surface of the semiconductor die.

3. (Previously presented) The semiconductor device package of claim 1, wherein the tape is formed from a material having a coefficient of thermal expansion similar to a coefficient of thermal expansion of a material of the semiconductor die.

4. (Previously presented) The semiconductor device package of claim 3, wherein the substrate element has a coefficient of thermal expansion similar to the coefficient of thermal expansion of the material of the semiconductor die.

5. (Previously presented) The semiconductor device package of claim 1, wherein both ends of the at least one slot formed through the tape extend beyond the outer periphery of the semiconductor die.

6. (Previously presented) The semiconductor device package of claim 1, wherein the tape is adhesively secured to the active surface of the semiconductor die and to the substrate element.

7. (Previously presented) The semiconductor device package of claim 1, wherein the substrate element comprises at least one of an interposer and a carrier substrate.

8. (Previously presented) The semiconductor device package of claim 1, wherein the substrate element comprises silicon.

9. (Previously presented) The semiconductor device package of claim 1, wherein the quantity of encapsulant material substantially encapsulates each intermediate conductive element.

10. (Previously presented) The semiconductor device package of claim 9, wherein the quantity of encapsulant material protrudes above a major plane of an exposed surface of the substrate element opposite the semiconductor die.

11. (Previously presented) The semiconductor device package of claim 1, wherein the substrate element includes a recessed area adjacent the at least one opening, each contact area of the plurality of contact areas being located within the recessed area.

12. (Previously presented) The semiconductor device package of claim 11, wherein the quantity of encapsulant material substantially fills the recessed area.

13. (Currently amended) The semiconductor device package of claim 12, wherein the quantity of encapsulant material substantially encapsulates each ~~the~~ intermediate conductive element.

14. (Previously presented) The semiconductor device package of claim 12, wherein the quantity of encapsulant material does not extend substantially beyond a major plane of an exposed surface of the substrate element.

15. (Cancelled)

16. (Previously presented) The semiconductor device package of claim 1, wherein the coverlay comprises a recessed area within which each intermediate conductive element is contained.

17. (Previously presented) The semiconductor device package of claim 1, wherein the coverlay is secured to the substrate element with an adhesive material.

18. (Previously presented) The semiconductor device package of claim 17, wherein the adhesive material comprises a pressure sensitive adhesive material.

19. (Cancelled)

20. (Previously presented) The semiconductor device package of claim 1, further comprising discrete conductive elements protruding from at least some of the contact pads.

21. (Previously presented) A semiconductor device assembly, comprising:
a semiconductor die with at least one bond pad on an active surface thereof;
a tape secured to the active surface, the tape including a slot formed therethrough with the at least one bond pad being exposed through the slot, at least one end of the slot extending beyond an outer periphery of the semiconductor die;
a substrate element positioned over the semiconductor die opposite the tape from the semiconductor die, the substrate element including at least one opening formed therethrough through which the at least one bond pad is exposed; and
a coverlay adhesively secured to a surface of the substrate element opposite the tape, the coverlay substantially covering at least the at least one opening through the substrate element.

22. (Previously presented) The assembly of claim 21, wherein the semiconductor die includes a plurality of bond pads arranged substantially linearly along a central region of the active surface.

23. (Previously presented) The assembly of claim 21, wherein the tape has a similar coefficient of thermal expansion to a coefficient of thermal expansion of the substrate element.

24. (Previously presented) The assembly of claim 23, wherein the semiconductor die has a similar coefficient of thermal expansion to the coefficient of thermal expansion of the substrate element.

25. (Previously presented) The assembly of claim 21, wherein two ends of the slot extend beyond the outer periphery of the semiconductor die.

26. (Previously presented) The assembly of claim 21, wherein the at least one end of the slot receives encapsulant material.

27. (Previously presented) The assembly of claim 25, wherein one of the two ends of the slot is positioned so as to facilitate displacement of air from the slot while an encapsulant material is being introduced at least into a volume defined by the slot from the other of the two ends.

28. (Previously presented) The assembly of claim 21, wherein the substrate element comprises at least one of an interposer and a carrier substrate.

29. (Previously presented) The assembly of claim 21, wherein the substrate element includes a recessed area formed adjacent the at least one opening in a surface of the substrate element located opposite the tape.

30. (Previously presented) The assembly of claim 29, wherein the substrate element includes at least one contact area corresponding to the at least one bond pad of the semiconductor die.

31. (Previously presented) The assembly of claim 30, wherein the at least one contact area is located within the recessed area.

32. (Previously presented) The assembly of claim 31, wherein the recessed area receives a portion of an intermediate conductive element that extends between the at least one bond pad and the at least one contact area.

33. (Previously presented) The assembly of claim 21, wherein the substrate element includes at least one contact area that corresponds to the at least one bond pad of the semiconductor die and at least one contact pad in electrical communication with the at least one contact area.

34. (Previously presented) The assembly of claim 33, further comprising at least one intermediate conductive element electrically connecting the at least one bond pad to the at least one contact area.

35. (Previously presented) The assembly of claim 34, wherein the at least one intermediate conductive element extends through the slot of the tape and the at least one opening of the substrate element.

36. (Cancelled)

37. (Previously presented) The assembly of claim 21, wherein the coverlay includes a recessed area configured to communicate with the at least one opening.

38. (Previously presented) The assembly of claim 37, wherein the recessed area is configured to receive a portion of at least one intermediate conductive element electrically connecting the at least one bond pad of the semiconductor die to a contact area on a surface of the substrate element adjacent the at least one opening formed therethrough.

39. (Previously presented) The assembly of claim 21, wherein the coverlay, the at least one opening formed through the substrate element, the slot formed through the tape, and the semiconductor die together form a receptacle.

40. (Previously presented) The assembly of claim 39, wherein the receptacle at least partially contains a quantity of encapsulant material.

41. (Previously presented) A method for packaging at least an active surface of a semiconductor die, comprising:

positioning a tape over the active surface so that at least one bond pad on the active surface is exposed through a slot formed through the tape and at least one end of the slot extends beyond an outer periphery of the semiconductor die;

positioning a substrate element over the tape so that the at least one bond pad is exposed through at least one opening formed through the substrate element and aligned with the slot, the substrate element including at least one contact area corresponding to the at least one bond pad;

electrically connecting the at least one bond pad to the at least one contact area;

adhesively securing a coverlay to an exposed surface of the substrate element to substantially cover the at least one opening formed through the substrate element; and

introducing encapsulant material through the at least one end into a receptacle formed by the coverlay, the at least one opening, the slot, and the semiconductor die from a location opposite the semiconductor die from the tape.

42. (Previously presented) The method of claim 41, wherein positioning the tape comprises positioning over the semiconductor die a tape having a similar coefficient of thermal expansion to a coefficient of thermal expansion of the semiconductor die.

43. (Previously presented) The method of claim 42, wherein positioning the substrate element comprises positioning over the tape a substrate element having a similar coefficient of thermal expansion to the coefficient of thermal expansion of the semiconductor die.

44. (Previously presented) The method of claim 43, wherein positioning the substrate element comprises positioning a substrate element comprising silicon over the tape.

45. (Previously presented) The method of claim 41, wherein positioning the tape comprises orienting the slot with another end thereof extending laterally beyond the outer periphery of the semiconductor die.

46. (Previously presented) The method of claim 41, further including securing the tape to the active surface of the semiconductor die.

47. (Previously presented) The method of claim 46, wherein securing comprises adhering the tape to the active surface.

48. (Previously presented) The method of claim 41, wherein positioning the substrate element comprises positioning at least one of an interposer and a carrier substrate over the tape.

49. (Previously presented) The method of claim 41, wherein positioning the substrate element comprises positioning over the tape a substrate element comprising a recessed area adjacent the at least one opening and including therein the at least one contact area.

50. (Previously presented) The method of claim 49, wherein introducing comprises introducing a portion of the encapsulant material into the recessed area.

51. (Previously presented) The method of claim 41, wherein electrically connecting comprises connecting at least one intermediate conductive element between the at least one bond pad and the at least one contact area.

52. (Previously presented) The method of claim 51, wherein connecting the at least one intermediate conductive element comprises wire bonding.

53. (Previously presented) The method of claim 51, wherein connecting the at least one intermediate conductive element comprises extending the at least one intermediate conductive element through the slot formed through the tape and the at least one opening formed through the substrate element.

54. (Currently amended) The method of claim 41, wherein ~~positioning~~ adhesively securing the coverlay comprises positioning over the substrate element a coverlay including a recessed area alignable over the at least one opening and over intermediate conductive elements extending through the at least one opening.

55. (Previously presented) The method of claim 41, further including securing the substrate element to the tape.

56. (Previously presented) The method of claim 55, wherein securing comprises adhesively securing the substrate element to the tape.

57. (Cancelled)

58. (Previously presented) The method of claim 41, wherein adhesively securing comprises securing the coverlay to the substrate element with a pressure sensitive adhesive.

59. (Previously presented) The method of claim 58, wherein adhesively securing comprises removably securing the coverlay to the substrate element.

60. (Previously presented) The method of claim 41, wherein introducing comprises substantially filling the slot formed through the tape and the at least one opening formed through the substrate element with the encapsulant material.

61. (Previously presented) The method of claim 41, wherein introducing comprises substantially encapsulating at least one intermediate conductive element electrically connecting the at least one bond pad to the at least one contact area.

62. (Currently amended) The method of claim 41, wherein ~~positioning~~ adhesively securing the coverlay comprises forming the receptacle, including the slot and the at least one opening, within which the at least one bond pad is located.

63. (Previously presented) A method for preparing a semiconductor die for packaging, comprising:

positioning a tape over at least an active surface of the semiconductor die, the tape including a slot through which at least one bond pad on the active surface of the semiconductor die is exposed, at least a portion of the slot extending laterally beyond an outer periphery of the semiconductor die;

positioning a substrate element over the tape with at least one opening formed through the substrate element being located at least partially over the slot; and

adhesively securing a coverlay to the substrate element to substantially seal the at least one opening, the coverlay and lateral edges of the at least one opening and the slot forming a receptacle.

64. (Previously presented) The method of claim 63, further comprising electrically connecting the at least one bond pad to at least one contact area located on a surface of the substrate element opposite the tape, proximate the at least one opening.

65. (Previously presented) The method of claim 64, wherein electrically connecting comprises connecting at least one intermediate conductive element between the at least one bond pad and the at least one contact area.

66. (Previously presented) The method of claim 65, wherein connecting the at least one intermediate conductive element comprises positioning the at least one intermediate conductive element at least partially within the slot and the at least one opening.

67. (Previously presented) The method of claim 63, wherein positioning the tape comprises positioning a tape having a coefficient of thermal expansion similar to a coefficient of thermal expansion of the semiconductor die.

68. (Previously presented) The method of claim 67, wherein positioning the substrate element comprises positioning over the tape a substrate element having a coefficient of thermal expansion similar to the coefficient of thermal expansion of the semiconductor die.

69. (Previously presented) The method of claim 63, wherein positioning the tape comprises positioning the tape with at least two regions of the slot extending laterally beyond the outer periphery of the semiconductor die.

70. (Previously presented) The method of claim 63, further comprising securing the tape to the active surface of the semiconductor die.

71. (Previously presented) The method of claim 70, wherein securing comprises adhesively securing the tape to the active surface of the semiconductor die.

72. (Previously presented) The method of claim 64, wherein positioning the substrate element comprises positioning over the tape a substrate element including a recessed area adjacent at least a portion of an edge of the at least one opening, the at least one contact area being located within the recessed area.

73. (Previously presented) The method of claim 63, wherein positioning the substrate element comprises positioning over the tape a substrate element comprising at least one of an interposer and a carrier substrate.

74. (Previously presented) The method of claim 63, further comprising securing the substrate element to the tape.

75. (Previously presented) The method of claim 74, wherein securing comprises adhesively securing the substrate element to the tape.

76. (Currently amended) The method of claim 63, wherein ~~positioning~~ adhesively securing the coverlay comprises positioning over the substrate element a coverlay comprising a recess formed therein, the recess being positioned so as to communicate with the at least one opening formed through the substrate element when the positioning is effected.

77. (Cancelled)

78. (Previously presented) The method of claim 63, wherein adhesively securing comprises adhesively securing the coverlay to the substrate element with a pressure sensitive adhesive.

79. (Currently amended) The method of claim 63, wherein adhesively securing comprises removably securing the coverlay to the substrate element.

80. (Previously presented) A semiconductor device package, comprising:

a semiconductor die with a plurality of bond pads arranged on an active surface thereof;

a tape positioned over the active surface, the tape including at least one slot formed therethrough, each of the plurality of bond pads being exposed through the at least one slot, at least one end of the at least one slot extending beyond an outer periphery of the semiconductor die;

a substrate element positioned over the tape opposite the semiconductor die, the substrate element including a plurality of contact areas, each contact area of the plurality corresponding to a bond pad of the plurality of bond pads and electrically connected thereto by way of an intermediate conductive element that extends through at least one opening formed through the substrate element and aligned with the at least one slot of the tape, the substrate element further including a contact pad in communication with each contact area of the plurality of contact areas by way of a substantially laterally extending conductive trace;

a quantity of encapsulant material substantially filling a volume defined by the at least one slot of the tape and the at least one opening of the substrate element; and

a coverlay positioned over a surface of the substrate element opposite the tape, the coverlay substantially covering at least the at least one opening through the substrate element, contact pads of the substrate element being exposed through or beyond the coverlay.

81. (Previously presented) The semiconductor device package of claim 80, wherein the plurality of bond pads is arranged substantially linearly along a central region of the active surface of the semiconductor die.

82. (Previously presented) The semiconductor device package of claim 80, wherein the tape is formed from a material having a coefficient of thermal expansion similar to a coefficient of thermal expansion of a material of the semiconductor die.

83. (Previously presented) The semiconductor device package of claim 82, wherein the substrate element has a coefficient of thermal expansion similar to the coefficient of thermal expansion of the material of the semiconductor die.

84. (Previously presented) The semiconductor device package of claim 80, wherein both ends of the at least one slot formed through the tape extend beyond the outer periphery of the semiconductor die.

85. (Previously presented) The semiconductor device package of claim 80, wherein the tape is adhesively secured to the active surface of the semiconductor die and to the substrate element.

86. (Previously presented) The semiconductor device package of claim 80, wherein the substrate element comprises at least one of an interposer and a carrier substrate.

87. (Previously presented) The semiconductor device package of claim 80, wherein the substrate element comprises silicon.

88. (Previously presented) The semiconductor device package of claim 80, wherein the quantity of encapsulant material substantially encapsulates each intermediate conductive element.

89. (Previously presented) The semiconductor device package of claim 88, wherein the quantity of encapsulant material protrudes above a major plane of an exposed surface of the substrate element opposite the semiconductor die.

90. (Previously presented) The semiconductor device package of claim 80, wherein the substrate element includes a recessed area adjacent the at least one opening, each contact area of the plurality of contact areas being located within the recessed area.

91. (Previously presented) The semiconductor device package of claim 90, wherein the quantity of encapsulant material substantially fills the recessed area.

92. (Currently amended) The semiconductor device package of claim 91, wherein the quantity of encapsulant material substantially encapsulates each ~~the~~ intermediate conductive element.

93. (Previously presented) The semiconductor device package of claim 91, wherein the quantity of encapsulant material does not extend substantially beyond a major plane of an exposed surface of the substrate element.

94. (Previously presented) The semiconductor device package of claim 80, wherein the coverlay comprises a recessed area within which each intermediate conductive element is contained.

95. (Previously presented) The semiconductor device package of claim 80, wherein the coverlay is secured to the surface of the substrate element.

96. (Previously presented) The semiconductor device package of claim 95, wherein the coverlay is secured to the surface of the substrate element with an adhesive material.

97. (Previously presented) The semiconductor device package of claim 96, wherein the adhesive material comprises a pressure sensitive adhesive material.

98. (Previously presented) The semiconductor device package of claim 80, further comprising discrete conductive elements protruding from at least some of the contact pads.

99. (Previously presented) A method for preparing a semiconductor die for packaging, comprising:

positioning a tape over at least an active surface of the semiconductor die, the tape including a slot through which at least one bond pad on the active surface of the semiconductor die is exposed, at least a portion of the slot extending laterally beyond an outer periphery of the semiconductor die;

positioning a substrate element over the tape with at least one opening formed through the substrate element being located at least partially over the slot; and

positioning a coverlay over the substrate element to substantially seal the at least one opening, the coverlay and lateral edges of the at least one opening and the slot forming a receptacle, contact pads at a surface of the substrate element adjacent to which the coverlay is positioned being exposed through or beyond an outer periphery of the coverlay.

100. (Previously presented) The method of claim 99, further comprising electrically connecting the at least one bond pad to at least one contact area located on a surface of the substrate element opposite the tape, proximate the at least one opening.

101. (Previously presented) The method of claim 100, wherein electrically connecting comprises connecting at least one intermediate conductive element between the at least one bond pad and the at least one contact area.

102. (Previously presented) The method of claim 101, wherein connecting the at least one intermediate conductive element comprises positioning the at least one intermediate conductive element at least partially within the slot and the at least one opening.

103. (Previously presented) The method of claim 99, wherein positioning the tape comprises positioning a tape having a coefficient of thermal expansion similar to a coefficient of thermal expansion of the semiconductor die.

104. (Previously presented) The method of claim 103, wherein positioning the substrate element comprises positioning over the tape a substrate element having a coefficient of thermal expansion similar to the coefficient of thermal expansion of the semiconductor die.

105. (Previously presented) The method of claim 99, wherein positioning the tape comprises positioning the tape with at least two regions of the slot extending laterally beyond the outer periphery of the semiconductor die.

106. (Previously presented) The method of claim 99, further comprising securing the tape to the active surface of the semiconductor die.

107. (Previously presented) The method of claim 106, wherein securing comprises adhesively securing the tape to the active surface of the semiconductor die.

108. (Previously presented) The method of claim 100, wherein positioning the substrate element comprises positioning over the tape a substrate element including a recessed area adjacent at least a portion of an edge of the at least one opening, the at least one contact area being located within the recessed area.

109. (Previously presented) The method of claim 99, wherein positioning the substrate element comprises positioning over the tape a substrate element comprising at least one of an interposer and a carrier substrate.

110. (Previously presented) The method of claim 99, further comprising securing the substrate element to the tape.

111. (Previously presented) The method of claim 110, wherein securing comprises adhesively securing the substrate element to the tape.

112. (Previously presented) The method of claim 99, wherein positioning the coverlay comprises positioning over the substrate element a coverlay comprising a recess formed therein, the recess being positioned so as to communicate with the at least one opening formed through the substrate element when positioning is effected.

113. (Previously presented) The method of claim 99, wherein positioning the coverlay includes securing the coverlay to the substrate element.

114. (Previously presented) The method of claim 113, wherein securing comprises removably securing the coverlay to the substrate element.

115. (Currently amended) The method of claim 113, wherein ~~adhesively~~ securing comprises removably securing the coverlay to the substrate element.

116. (Previously presented) The assembly of claim 21, wherein the coverlay is secured to the surface of the substrate element with an adhesive material.

117. (Previously presented) The assembly of claim 116, wherein the adhesive material comprises a pressure sensitive adhesive material.

118. (Previously presented) The assembly of claim 21, wherein the coverlay is removably secured to the surface of the substrate element.